

(SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2023	(Semester)	2	(Course No.)	2150084301
(Class)	01	(Open to)		(Course Classification)	-
(Credit)	3.0		03		100
(Office)	051306	(Telephone)	02-820-0710	(e-mail)	chlee@ssu.ac.kr
	(FL), (PBL)		+		
	(*) (ABEEK Classification)		(*) (ABEEK Requirement)		
	(C),				
(Course Description)	, CAD tool , HDL(Hardware Description Language)				

Verilog HDL	

가	(100)	(100%)
	100	100

(Required Texts)		* /Digital System Designs and Practices////Ming-Bo Lin/Wiley/2008/
	()	* /HDL SOC IP / / /2004/ * /Starter's guide to Verilog 2001/M Ciletti/Pearson/2004/
	:	(C)
	Engaged learning : 50%, 15%, 25%, 10%	

2.

(Week)	(Keyword)	(Description)		(Texts)
--------	-----------	---------------	--	---------

(SYLLABUS)

01		HDL		,
02	Verilog HDL	Verilog HDL syntax.		,
03	Dataflow			,
04	Simulation	Verilog HDL S/W , simulation , Testbench	, , ,	,
05	Behavioral	Behavioral H/W	,	,
06	Behavioral	Behavioral ,	,	,
07	Behavioral	Behavioral .	,	,
08		: microprocessor/FIR filter .	, ,	,
09	FSM	Finite state machine - state diagram, :	, , , , , ,	,
10	FSM	Finite state machine - ASM chart, :	, , , , , ,	,
11	, task,	Verilog HDL system task . :	, ,	,
12		()		11/18() 1:00 – 3:30
13	RTL(Register Transfer Level)	RTL(Register Transistor Level) , :	, ,	,
14	Design example	Design example: Combinational logic, :	, ,	
15	Design example	Design example: sequential logic,	, ,	

(SYLLABUS)

[]

65 2
,
가

,가

가

[]

:
:
:
:
/
:
/

[가]

/ / :
/
:
가

(02-820-0060)

(SYLLABUS)

3. ()

()			
	가/		
	/		
	/		
	/		
	Open-ended problem		
	Teamwork		
	Communication skills		